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semiconductor and (trench or groove) and pad and mask and etch	6

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DATE: Thursday, May 30, 2002   Printable Copy   Create Case

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L1	semiconductor and (trench or groove) and pad and mask and etch	102	L1
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L2	semiconductor and (trench or groove) and pad and mask and etch	6	L2
	DB=USPT; PLUR=YES; OP=ADJ		
L3	semiconductor and (trench or groove) and pad and mask and etch	3054	L3
	DB=PGPB; PLUR=YES; OP=ADJ		
L4	semiconductor and (trench or groove) and pad and mask and etch	447	L4
	DB=JPAB; PLUR=YES; OP=ADJ		
L5	semiconductor and (trench or groove) and pad and mask and etch	3	L5
	DB=EPAB; PLUR=YES; OP=ADJ		
L6	semiconductor and (trench or groove) and pad and mask and etch	6	L6

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Search Results - Record(s) 1 through 6 of 6 returned.

☐ 1.   Document ID: NN9412475

L2: Entry 1 of 6   File: TDBD   Dec 1, 1994

TDB-ACC-NO: NN9412475

DISCLOSURE TITLE: New Etch Process for Luna ES1 Shallow Trench Isolation (IT Etch)

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, December 1994, US

VOLUME NUMBER: 37
ISSUE NUMBER: 12
PAGE NUMBER: 475 - 476

PUBLICATION-DATE: December 1, 1994 (19941201)

CROSS REFERENCE: 0018-8689-37-12-475

DISCLOSURE TEXT:

This document contains drawings, formulas, and/or symbols that will not appear on line. Request hardcopy from ITIRC for complete article. Disclosed is a dry etch process designed to improve the quality of the shallow trench isolation for advanced semiconductor products such as 16 Mbits DRAM chips. This new process uses a low pressure NF3/N2/CHF3 chemistry - when the conventional NF3/N2 chemistry is used, four main defects have been detected as illustrated in Fig. 1: o Nitride node remainings, o Possible negative profiles, o Mask deformation (wafer edge), o Possible Pad Nitride erosion (wafer edge).

A new NF3/N2/CHF3 chemistry is disclosed to avoid these defects. First, the use of an additional CHF3 flow leads to a thin polymer deposition along the etched surfaces. This thin layer protects the Isolation Trench (IT) profiles against lateral etching, avoiding negative profiles. Next, changing NF3/CHF3 ratio allows an IT slope and center-to-edge depth uniformity control. CHF3 increases nitride etch rate, so that nitride nodes are etched faster than silicon and polysilicon and eliminated. CHF3 decreases resist etch rate: etch-bias and dimensionnal are more stable. New IT profile leads to a better oxyde fill, which in turn, improve IT isolation and reduces the number of dislocations.

Electrical parameters related to IT have shown a clear improvement on wafers processed with new plasma parameters as illustrated in Fig. 2.

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc |

☐   2.   Document ID: NN881261

DISCLOSURE TEXT:

- This article describes a self-alignment scheme for heterostructure bipolar junction transistors that allows reduction and reproducible production of base-emitter and base-collector junctions, passivation of surfaces and interfaces, removal of non-annealed ion-implantation damage from active region and reduction in mask steps involved in fabrication of these devices. More specifically, a self-alignment scheme also is described for a planar bipolar junction transistor. High-speed heterostructure bipolar junction transistors require suppression of both parasitic capacitances and resistances. Processing procedures similar to those described here can be used for making all heterobipolar transistors in other heterostructure technologies. Examples of these would be InAlAs/InGaAs, GaP/Si, Si/SiGe, silicon polyoxide semiconductor Si, InP/InGaAs, etc. Similar procedures could be incorporated in homostructure technologies, provided the underlying speed-design trade-offs are useful. For the purposes of the discussion here, we will use the example of a GaAlAs/GaAs system. In this heterostructure system, it can be shown that diffusion capacitances are only a small component of the overall non-saturating logic delays. Under such conditions, making devices extremely small, maintaining low resistances with the above and vertical scaling are extremely important. In addition, generation-recombination centers introduced during implantation steps have to be removed from active device regions to enable useful bipolar action. Also, the processes need to be simplified using self-alignment to make technology reproducible for manufacturing. ***** SEE ORIGINAL DOCUMENT ***** The structure evolves from a sensitivity analysis and detailed simulation of relative effect of base resistance and base collector capacitance in transistor performance and emitter-coupled logic (ECL) circuit delays. It is seen that, since the base dopings allowed in heterostructure bipolar transistor (HBT) structures are high (greater than 1E19 cm-3 for GaAlAs/GaAs system), one base contact instead of two base contacts raises the unloaded and loaded (FI=3, FO=3, C=0.1 pF) in 1 micron design rule structures from 20 and 56 to 24 and 62 pS at low 10E4 A/cm2 current density. However, if this reduction in contact area is utilized in reducing the collector-base junction area, the corresponding reductions outweigh the increase. With one base contact and collector contact at 1 micron rules, unloaded and loaded delays of 17 and 47 pS occur under similar current density. Use of self-alignment for registration reduces these delays further. The projected delays for devices using the self-alignment of this disclosure reduces these delays to sub-15 and sub-40 pS range. One embodiment is shown in Fig. 1. Other embodiments also are described to allow other structural forms using these same principles. The process is described for a double heterostructure transistor, with the conventionally used dopings, heavy doping (>1E18 cm-3) for the n-type GaAs contact and sub-collector layer, (>5E18 cm-3) for the p- type GaAs base, and near 1E17 cm-3 for the GaAlAs emitter and collector. Variation of these processing procedures, but a similar structure, allows the fabrication of a Schottky clamped collector up structure for Schottky transistor logic (STL)-type applications. ***** SEE ORIGINAL DOCUMENT ***** Referring to Figs. 2 through 10, the process to fabricate the device is set forth as follows: Step 1: The material structure is grown, INS1 (an insulator level, e.g., Si3N4) is deposited by a technique such as plasma-enhanced chemical vapor deposition (PECVD). A double-layer photoresist (PR) (e.g., 3000 PR/poly-methyl methacrylate) is used to define the region for top emitter contact (Fig. 2). Step 2: Using reactive ion etch (RIE), the INS1 is removed followed by removal of the top contact layer of the structure into the wider band-gap material. The wider band-gap material may be completely removed to expose the base layer. Either RIE or wet chemical etching may be employed for removal of the semiconductors (Fig. 3). Step 3: The top (PR) layer is removed, and a second insulator (INS2) formed on the structure. One example is deposition of Ta followed by anodization, another is deposition of SiO2 by conformal

means, such as sputtering or PECVD. The INS2 is selected for its selectivity towards etching with respect to INS1 and INS3 that follows in a later step (Fig. 4). ***** SEE ORIGINAL DOCUMENT ***** Step 4: The INS2 is RIE etched and the under-layer resist removed. This leaves two collars on the side of the emitter mesa structure. This is followed by formation of the self-aligned p+ contact region. This can be done either by an acceptor (such as Mg, Zn, Cd, etc.) implantation followed by annealing or by diffusion from vapor or solid source (e.g., Zn from Zn2As3). Diffusion may be preferable because it leaves less number of generation-recombination centers (Fig. 5). Step 5: Using the collars and INS1 as a mask with photoresist overlay to define the base contact and alignment region, etch away the excess p+ region. The etching may also remove the lower doped collector (nGaAlAs) to allow contact to the higher doped sub-collector and may be done either by RIE or wet etching (Fig. 6). ***** SEE ORIGINAL DOCUMENT ***** Step 6: Deposit by a conformal process INS3 after removing the resist. INS3 may be Si3N4 deposited by PECVD and should have similar behavioral characteristics as INS1 (Fig. 7). Step 7: Mask with PR to define the base contact pad, deposit the base contact metallurgy (e.g., AuZn, AuBe, AuMg etc.), lift-off and sinter to form the contact (Fig. 8). Step 8: Using photoresist mask, open emitter and collector contact regions by RIE of the INS3 and INS1. INS2 acts as a selective mask for this RIE process (e.g., in FREON* 14:H2, or FREON 14 process, etc.). Deposit metallurgy for the two by lift-off and alloy (e.g., AuGe) to form the ohmic contact (Fig. 9). Step 9: Use another masking level to define isolation implant region. The lateral region of the bipolar structure is protected by the INS2 and INS3 collar, the base contact side by either the INS3 collar or by a photoresist extending beyond, and the collector side by the collector metallurgy or the photoresist extending beyond (Fig. 10). There are several variations on these processing procedures that allow optimal construction of a device for different technological approaches. Some of these are described below. ***** SEE ORIGINAL DOCUMENT ***** 1. The base, emitter, and collector metallurgy may be selected to be the same (e.g., AuGe/Ni/Au) by increasing the surface doping of the p+ region formed to high 10E19 cm-3 or above range. This reduces the mask steps to a bare 4 from an already low count of 5. These masking steps are shown as a variation on Step 6 in Figs. 11A and 11B. 2. The structure could be made relatively planar by introducing a regrowth step for the collector contact using the INS3 as a mask, or by introducing an implantation step for contacting the subcollector after forming a groove to isolate the heavy doped base from this implant. This groove may be 1 micron wide and used to reduce leakage currents at the base-collector junction (Figs. 12 and 13). In addition, Fig. 14 shows how depositing a thick metallurgy for collector contact can also be used as a means of avoiding problems related to large step heights. 3. Base contact metallurgy and collector contact metallurgy can be self-aligned by following, after Step 6, a deposition of the INS2- type metallurgy and RIE to form the collars for the base and one of the collars for the collector. This is followed by metallizations of the appropriate metallurgies as before. Figs. 11A and 11B show this sequence, which can be used in addition to the already defined step to bring the base and collector contact closer. The major advantage of this technique is in reducing the base junction area further by allowing aligning the outside edge of the contact. ***** SEE ORIGINAL DOCUMENT ***** 4. Oxygen implantation with the acceptor implant allows a semi- insulating region to be formed underneath the p+ region, allowing for a lower base-collector capacitance. 5. Emitter and collector contacts can be interchanged to allow for a collector up mode of operation with large gains. 6. The same structure can be used with a single heterostructure technology to make a single heterostructure device. 7. A smaller base contact could be formed with additional complexity introduced in processing allowing for subtractive etching for the base contact similar to the emitter contact using one of the collars of the emitter contact. The collector contact itself does not contribute to capacitance and thus need not be made close-spaced or small-dimensioned. An advanced structure that reduces base contact, base junction area and planarizes the transistor structure is shown in Fig. 15. The fabricated device can be operated both in upward and downward direction with useful gain because it uses a double heterostructure. Of course, single heterostructures can be used, with emitter up or emitter down. Technology can also be applied to all bipolar and unipolar hot electron structures. These structures derive their advantage from high speed due to low capacitance, use of a single base contact to reduce device dimension and ease of manufacturability from self-aligning and planarizing. The processes described reduce device dimensions to the bare minimum from resolution of lithography to registration limited by self-aligning. A typical process sequence as illustrated in Figs. 16 through 24 is as follows: 1. Grow material and deposit INS1 (e.g., Si3N4) and form a double-layer lithography structure (e.g., PR/PMMA) (Fig. 16). 2. RIE INS1, contact GaAs layer into GaAlAs (the second step could be a wet etch) (Fig. 17). 3. Remove top resist, deposit a second insulator INS2, which can be selectively etched with respect to INS1 (examples are Ta205 on SiO2, etc.) (Fig. 18). 4. RIE INS2 to form collar, and form p+ region for base contact. The second resist could be removed before or after implant. For diffusion, it is removed before (Fig. 19). 5. Define base area, etch into collector layers using one of insulator edges for collector edges alignment. Base

area should be kept near the resolution limit (Fig. 20). 6. Deposit INS3 which is selective like INS1 with INS2. RIE to form collars (Fig. 21). 7. Deposit a planarizing layer (e.g., polyimide, cured) and planarize (Fig. 22). 8. Form Emitter, base and collector contacts. It may be possible

to E and C in same step because of similar polarity. To make contact to collector, use RIE to etch to n+GaAs (Fig. 23). 9. Isolation-implementing ohmic edges or PR edges or mask with PR over device and, insulators for edge protection and interconnect (Fig. 24). Alternatively, the base contact edge collar could also be used for isolation, as shown in Fig. 15. * Trademark of E. I. du Pont de Nemours & Co.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments		KWIC	Draw Desc	Clip Img

☐ 3. Document ID: NN8804448

L2: Entry 3 of 6   File: TDBD   Apr 1, 1988

TDB-ACC-NO: NN8804448

DISCLOSURE TITLE: Polish Stop Structure for Oxide-Filled Semiconductor Trenches

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, April 1988, US

VOLUME NUMBER: 30
ISSUE NUMBER: 11
PAGE NUMBER: 448 - 449

PUBLICATION-DATE: April 1, 1988 (19880401)

CROSS REFERENCE: 0018-8689-30-11-448

DISCLOSURE TEXT:

- A process is disclosed for using a refractory metal and/or refractory silicide as a planarization polish stop for polishing oxide materials used to fill shallow isolation trenches fabricated in the CMOS technology. Silicon dioxide is the obvious choice of insulators to use for filling shallow isolation trenches. Unfortunately, polishing processes do not work well for structures wherein the polish step is intended to remove oxide, due to a poor polish rate ratio between oxide and nitride (etch stop). This leads to cross-wafer uniformity problems, difficulties in removing oxide over large untrenched regions, and end point detection problems. The following structure requirements should be considered when replacing nitride as the polish stopping film for oxide filled trenches: 1) A proper reactive ion etch (RIE) mask material should be provided on top of the structure when forming trenches. The mask material of choice for most RIE trenching processes is silicon dioxide. 2) Because thermal oxide is grown on the side walls of newly formed trenches to remove any RIE damage to the silicon, the RIE mask material should protect active device regions from oxidation during thermal oxide growth. 3) The mask material should not be attacked by acids used to remove sacrificial silicon dioxide films on trench sidewalls. 4) The mask should polish slowly relative to the trench fill. 5) Mask stripping must not damage the underlying active regions or the trench fill. A new masking structure is shown in Fig. 1 composed of a thin thermal oxide pad 10 on a silicon substrate 11, a refractory metal or a refractory metal silicide 12, in combination with a polysilicon layer 13 to enhance oxidation, and a silicon dioxide capping layer 14. The refractory metal or silicide 12 is employed as a polish resistant layer (etch stop) to protect the underlying single crystal regions from oxidation during trench sidewall passivation. A silicon dioxide cap 14 is employed as a mask for the shallow isolation trench RIE. To form the stack structure shown in Fig. 1, a thermal oxide pad 10-25nm thick is formed on top of the silicon substrate. A refractory metal silicide film with a polysilicon layer (polycide) may be chosen over a refractory metal because polycides behave well under most oxidation conditions. The thickness of the refractory layer is determined by the relative polish rates of it to the oxide fill used in the shallow isolation trench. A chemical vapor deposition (CVD) of silicon dioxide forms a cap approximately 300 nm thick on top of the structure is utilized as a RIE mask. The isolation trench pattern is defined

using conventional photolithographic techniques. Fig. 2 shows the structure after a RIE through the oxide/refractory/oxide stack 15 is performed and the resist is stripped. Fig. 3 shows the trench 16 formed by a RIE. The trench sidewalls are passivated with a thermal oxide 17. Optionally, nitride 18 may be deposited as a further sidewall passivation layer. The trench is filled (not shown) with CVD silicon dioxide or nitride. The fill material is then polished, stopping on the refractory metal. Finally, the refractory layer and the underlying pad are removed using conventional methods. At this point the structure is ready for the formation of active devices.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments		KWIC	Draw Desc	Clip Img

☐ 4. Document ID: NN88018

L2: Entry 4 of 6   File: TDBD   Jan 1, 1988

TDB-ACC-NO: NN88018

DISCLOSURE TITLE: Process for Fabricating Submicron Resistors With the Base Poly- Silicon

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, January 1988, US

VOLUME NUMBER: 30
ISSUE NUMBER: 8
PAGE NUMBER: 8 - 9

PUBLICATION-DATE: January 1, 1988 (19880101)

CROSS REFERENCE: 0018-8689-30-8-8

DISCLOSURE TEXT:

- Submicron resistors for semiconductors are formed by using base polysilicon (PolySi) for the sidewall formation. The proposed method requires less process steps than existing methods and also includes resistors in silicon with high-dimensional control. Using the sidewall image transfer technique, as shown in Fig. 1, a layer 1 of PolySi doped with boron is deposited over an oxide 2/nitride 3 layer laid down on an Si substrate 4. The oxide/nitride layer was defined using a reactive ion etch (RIE) of the nitride plus most of the oxide with a wet etch of the remaining $SiO2$. The $Si3N4$ was introduced for applications where p+ PolySi is allowed to overlap the deep trench isolation. The dual-dielectric concept is known to prevent shorts between conducting layers. ***** SEE ORIGINAL DOCUMENT ***** The PolySi of Fig. 1 receives an RIE using $CCl2F2$ with a 30% over- etch. Pads at the G level 5 (Fig. 2) will overlap ends of the F level 6, as seen in the top view. After the RIE, PolySi rails 7, shown in Figs. 2 and 3, are formed over the oxide 2/nitride 3 topography. The rails 7 are in intimate contact with the PolySi pads as defined by the G level mask. The contact to the PolySi pads is made later in the processing operation with no additional masking steps. The G level pads are used to contact the PolySi resistor.

☐ 5. Document ID: NN87024056

L2: Entry 5 of 6   File: TDBD   Feb 1, 1987

TDB-ACC-NO: NN87024056

DISCLOSURE TITLE: CMOS Isolation by Use of a Floating, Self-Aligned N+ Guard Ring Around the N-Well

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, February 1987, US

VOLUME NUMBER: 29
ISSUE NUMBER: 9
PAGE NUMBER: 4056 - 4057

PUBLICATION-DATE: February 1, 1987 (19870201)

CROSS REFERENCE: 0018-8689-29-9-4056

DISCLOSURE TEXT:

- A simplified method has been proposed to prevent latch-up in complementary metal-oxide-semiconductors (CMOS) which integrates a guard ring into the CMOS isolation process of a semi-ROX (recessed oxide) structure. The methodology involves the superimposing of an N+ guard ring around the N-well of the P-channel device. A lift-off embodiment of the N-well mask is used which utilizes a multi-level resist 1 (Fig. 1) with the bottom layer being polyimide. After pad oxidation 4 and Si3N4 deposition 3, the N-well 2 can be implanted. Following the implant, Al 6 is deposited over the structure (Fig. 2). The Al will be thinner and etch faster over the vertical ***** SEE ORIGINAL DOCUMENT ***** edges of the resist mask, and a dip-etch will etch back the Al to the configuration shown in 5, which results in a gap 7 created by the etch-back. In the next step, N+ for the self-aligned guard ring 8 can be implanted (Fig. 3). It will only go into the Si at the edges of the N- well 2, where the gaps 7 were created by the Al etchback. Following this, lift-off is performed and ROX level resist used and aligned to the Al pattern left after the N-well formation. ROX resist is used to pattern the Si3N4 and as an implant mask for the P type field implant. This method involves no extra masks since it is self-aligned and is much simpler to use as compared with other methodologies, such as trench isolation, which are more complex.

☐ 6. Document ID: NN8607943

L2: Entry 6 of 6   File: TDBD   Jul 1, 1986

TDB-ACC-NO: NN8607943

DISCLOSURE TITLE: Reduced Bird's Beak ROI Process

PUBLICATION-DATA:

IBM Technical Disclosure Bulletin, July 1986, US

VOLUME NUMBER: 29
ISSUE NUMBER: 2
PAGE NUMBER: 943 - 946

PUBLICATION-DATE: July 1, 1986 (19860701)

CROSS REFERENCE: 0018-8689-29-2-943

DISCLOSURE TEXT:

- Disclosed is a process for reducing the length of "bird's beak" associated with a recessed oxide isolation (ROI) region of semiconductor devices. The process uses phosphorous-doped polysilicon to achieve a rapid oxidation which lends itself to a reduced bird's beak. Referring to Fig. 1, starting with an N-Si, a thin layer of thermal oxide 2 and a layer of silicon nitride 3 are formed. The device region in the form of pedestal 1 is defined by reactive ion etching a trench. Then, another oxide layer 2' is grown in the trench. This oxide 2' will prevent any dopant in the subsequently deposited doped polysilicon layer from diffusing into the silicon. Silicon nitride 3 serves as an oxidation mask. Referring to Fig. 2, next, phosphorous-doped polysilicon 4 having a N+ content equal to or exceeding the solid solubility limit is deposited. The thickness of the polysilicon 4 is controlled to be equal to or thicker than the step height: Tpoly = Tox + Tnitride + Tsi etch The wafer surface is next planarized as shown in Fig. 3. The nitride layer 3 on the silicon pedestal 1 serves as a polish stop. The remaining polysilicon is then thermally oxidized in steam to form the recessed oxide having a bird's beak 5 (Fig. 4) of a length dictated by the oxidation temperature, as indicated in the table below. The nitride 3 and oxide 2 are removed to expose the Si surface for further processing. Bird's Beak Length As Related To Oxidation Temperature(1,2) A schematic representation of the concept is indicated in Fig. 5, wherein the oxidation of polysilicon takes place in three steps. Initially, oxidation of the top polysilicon 4, with a thickness equal to the mask nitride layer 3, produces an oxide with essentially no bird's beak. This is because there is no path for lateral diffusion of oxygen into the Si. This thickness of oxide 6 is about 2.2 times that of the nitride 3 thickness. As the oxidation proceeds to consume the next layer of polysilicon, a small bird's beak 7 will be formed with its thickness equal to the thin pad oxide 2. The length of the bird's beak is negligible. The next step, which is the oxidation of the remaining polysilicon below the level of the pad oxide, is analogous to the semi-ROI process. Since this proceeds at a rate considerably faster than does the lateral oxidation of N-crystal Si, the bird's beak length 5 will be considerably shorter than that of a standard semi-ROI. The oxidation rate ratio will be dependent upon temperature, as previously indicated in the table.

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC | Draw Desc | Clip Img |

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Terms	Documents
semiconductor and (trench or groove) and pad and mask and etch	6

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Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1.   Document ID: JP 2000031502 A

L5: Entry 1 of 3   File: JPAB   Jan 28, 2000

DOCUMENT-IDENTIFIER: JP 2000031502 A
TITLE: MANUFACTURE OF SEMICONDUCTOR DYNAMIC QUANTITY SENSOR, AND SEMICONDUCTOR DYNAMIC QUANTITY
SENSOR

Abstract (2):
SOLUTION: The basic structure of a semiconductor acceleration sensor 1 is completed, by (a)
preparing an SOI substrate 14, where a single crystal silicon film 14b is provided through a
silicon oxide film 14c on a single crystal silicon wafter 14a, and then, by executing an
electrode pad formation process (b) which forms electrode pads 4c and 5c, a dimension adjustment
process (c) which grinds and polishes a single crystal silicon film 14b, a mask formation
process (d) which forms a mask 15, a trench formation process (e) which forms a trench 16
reaching a silicon oxide film 14c in a single crystal silicon film 14b, a first etching process
(f) which wet etches the single crystalline silicon wafer 14a, leaving a specified thickness, a
second etching process (g) which removes the above remaining single crystal silicon wafer 14a by
dry etching, and a third etching process (h) which removes the silicon oxide film 14c by dry
etching.

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC | Draw Desc | Image |

☐ 2.   Document ID: JP 11284141 A

L5: Entry 2 of 3   File: JPAB   Oct 15, 1999

DOCUMENT-IDENTIFIER: JP 11284141 A
TITLE: METHOD FOR FORMING INTEGRATED CIRCUIT

Abstract (1):
PROBLEM TO BE SOLVED: To reduce an erosion of a pad during manufacturing a semiconductor by a
method wherein a pad stack is formed on a substrate, and a hard mask comprising a first hard
mask, an etch stop layer and a second hard mask layer is formed on the pad stack.

Abstract (2):
SOLUTION: On a substrate surface, a pad stack layer 310 comprising a pad oxide film layer 312
and a pad stop layer 314 is formed and further a pad stop layer 312 as a pad nitride is formed.
A hard mask layer 315 has an etch stop 318 between a first hard mask 316 and a second hard mask
320. And, the first hard mask 316 and the second hard mask 320 are composed of a material having
minuteness or stiffness which sufficiently endures a collision of ions by RIE during a deep
trench formation. Further, the etch mask has a wet etch rate higher than the pad etch stop
layer.

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC | Draw Desc | Image |

☐   3.   Document ID: JP 62069639 A

L5: Entry 3 of 3   File: JPAB   Mar 30, 1987

DOCUMENT-IDENTIFIER: JP 62069639 A
TITLE: MANUFACTURE OF SEMICONDUCTOR DEVICE

Abstract (1):
PURPOSE: To reduce the steps constituting a photolithographic process and thereby to simplify said process by a method wherein a mask used in removing a first layer also serves as a mask in implanting channel stopper ions.

Abstract (2):
CONSTITUTION: A pad SiO2 11 and silicon nitride layer 12 are formed on a semiconductor substrate 1, and three layers of silicon nitride/pad SiO2/Si are subjected to etching for the formation of grooves 21a, 21b, and 22. Next, a first layer 41 and resist 61 are formed by photolithography on the substrate 1, etching is accomplished for the removal of the first layer 41 in a region 31a, and N-channel stopper ions 51 are driven into the groove internal surfaces. A P-channel first layer is subjected to etching, P-channel stopper ions 52 are driven into the groove internal surfaces, the resist 61 is removed, and a second layer 42 is formed on the first layer retained in the grooves and on the entire surface of the substrate 1. A layer 6 is formed, an etch-back process follows wherein the SiO2 second layer and layer 6 are etched at the same rate. The layers 12 and 11 are removed for the completion of isolation between elements.

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC | Draw Desc | Image |

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Terms	Documents
semiconductor and (trench or groove) and pad and mask and etch	3

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Search Results - Record(s) 1 through 6 of 6 returned.

☐   1.   Document ID: US 5684319 A

L6: Entry 1 of 6   File: EPAB   Nov 4, 1997

DOCUMENT-IDENTIFIER: US 5684319 A
TITLE: Self-aligned source and body contact structure for high performance DMOS transistors and method of fabricating same

Applicant Name (1):
NAT SEMICONDUCTOR CORP

Applicant Name (Derived) (1):
NAT SEMICONDUCTOR CORP

Abstract (1):
A DMOS device structure, and method of manufacturing the same features a self-aligned source and body contact structure which requires no additional masks. Polysilicon spacers are used to form the source region at the periphery of the gate polysilicon. The preferred method of manufacturing uses five masks to produce a discrete DMOS semiconductor chip. An N- epitaxial layer is grown on an N+ substrate. Thick field oxide is grown. A first mask is used to etch an active region. Thin gate oxide is grown. Doped polysilicon is then deposited. A second mask is used to etch the polysilicon, thereby forming the gates. Insulating oxide is grown. A blanket P body implantation is performed. A thermal drive-in step laterally and vertically diffuses the implanted P type impurity throughout body regions. The insulating oxide is etched. A polysilicon layer is deposited and doped. A dry etch leaves polyslicon spacers along the edges of the gates. A P+ body contact implantation is performed, thereby forming body contact regions. A final annealing step causes vertical and lateral out-diffusion of the N type dopant from the N+ spacers down into substrate to form source N+ regions which partially underlie the gate polysilicon. A third mask is used to etch a gate contact area on a segment of the polysilicon above the field oxide. Metal is deposited, and a fourth photoresist mask delineates a gate pad region and a source pad region which also extends over the source contacts. A passivation layer is deposited and etched in the source and gate pad regions using a fifth mask. In another embodiment, a trench DMOS transistor is fabricated using an additional mask to guide a dry etch to "dig" the trenches.

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC | Draw Desc | Image |

☐   2.   Document ID: US 5424240 A

L6: Entry 2 of 6   File: EPAB   Jun 13, 1995

DOCUMENT-IDENTIFIER: US 5424240 A
TITLE: Method for the formation of field oxide film in semiconductor device

Abstract (1):
A method for the formation of field oxide film in a semiconductor device is disclosed. The method comprises the steps of: forming a first nitride film on a silicon substrate, the silicon

substrate being previously covered with a pad oxide film; applying etch to the nitride film, the pad oxide film and the silicon substrate in due order, so as to form a trench in a predetermined portion; depositing a polysilicon film entirely on the resulting structure, so as to cover the trench and the nitride film; subjecting the polysilicon film to planarization; forming a second nitride film on the plane polysilicon film and etching back the second film, so as to form a spacer nitride film at either side wall of the first nitride film; etching the plane polysilicon film filling the trench, so as to expose a predetermined portion of the trench, the spacer nitride film and the first nitride film being used as an etch mask; forming a field oxide film in the trench by use of an oxidation process and removing the first nitride film, the spacer nitride film and the pad oxide film. The method is preventive of the stress on silicon substrate and the occurrence of defective in device, whereby highly integrated devices can be fabricated.

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC | Draw Desc | Image |

☐ 3. Document ID: US 5411913 A

L6: Entry 3 of 6   File: EPAB   May 2, 1995

DOCUMENT-IDENTIFIER: US 5411913 A
TITLE: Simple planarized trench isolation and field oxide formation using poly-silicon

Applicant Name (1):
NAT SEMICONDUCTOR CORP

Applicant Name (Derived) (1):
NAT SEMICONDUCTOR CORP

Abstract (1):
A device isolation scheme that is particularly suited to the fabrication of high density, high performance CMOS, bipolar, or BiCMOS devices, and overcomes many of the problems associated with existing isolation methods. Photolithographic techniques are used to define active regions on a substrate. Using the photoresist as a mask for the active regions, the silicon in the inactive regions is etched. A pad oxide layer and nitride layer are then formed on the substrate. A layer of oxide is then deposited and photolithographic techniques are again used to define the locations for desired trench structures. After removal of the remaining photoresist, deep trenches are etched in the silicon substrate. An oxidation step is then carried out to provide a layer of oxide lining the trenches, followed by deposition of a layer of poly-silicon over the substrate, filling the trenches. The poly-silicon layer is etched back, removing it from the tops of the trenches and the field regions, and leaving a poly-silicon spacer on the sides of those portions of the previously deposited oxide layer which cover the active regions. The spacers are used to align a photoresist mask which is used to etch away the oxide layer on top of the active regions. The spacers are then removed while keeping the photoresist mask intact, thereby protecting the poly-silicon on top of the trenches. The photoresist mask is then removed and the poly-silicon on top of each trench is oxidized to cap the trench. The result is a highly planar surface in which active regions are separated by field oxide or poly-silicon filled trenches.

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC | Draw Desc | Image |

☐ 4. Document ID: EP 562127 A1

L6: Entry 4 of 6   File: EPAB   Sep 29, 1993

DOCUMENT-IDENTIFIER: EP 562127 A1
TITLE: METHOD FOR FABRICATION OF SEMICONDUCTOR DEVICE.

Abstract (1):
This invention is directed to prevent step breakage and short-circuit of wires resulting from steps of isolation trenches formed in an SOI substrate. An oxide film for a pad is formed on a main plane of an SOI layer formed on an insulating substrate and furthermore, a silicon nitride film and an SiO2 film are sequentially formed. Thereafter, isolation trenches reaching the insulating substrate are formed by RIE using the SiO2 film as the mask. An insulating film is then formed on the inner wall of the isolation grooves by thermal oxidation, and polycrystalline silicon is filled into the insolation trenches. This polycrystalline silicon is etched back while control is made so that the upper end of polycrystalline silicon inside the isolation trenches is above the upper end of the silicon nitride film, and the excessive polycrystalline silicon deposited on the substrate surface is removed. Next, polycrystalline silicon inside the isolation trenches and the silicon nitride film are used as an etching stopper to etch and remove the SiO2 film used as the mask at the time of the formation of the isolation trenches. Since this etching and removal of the SiO2 film used as the mask is carried out after polycrystalline silicon is filled into the isolation trenches, the oxide film for isolating the substrates inside the SOI substrate is not etched when the mask is removed. When the masking SiO2 film is etched and removed, polycrystalline silicon and the silicon nitride film inside the isolation trenches function as the etching stopper, and the oxide film for the pad as the lower layer and the insulating film formed on the inner wall of the trenches are prevented from being etched, and flatness in the trench portions is not lost.

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC | Draw Desc | Image |

☐ 5. Document ID: US 5217919 A

L6: Entry 5 of 6   File: EPAB   Jun 8, 1993

DOCUMENT-IDENTIFIER: US 5217919 A
TITLE: Method of forming island with polysilicon-filled trench isolation

Abstract (1):
A process of manufacturing a trench-isolated semiconductor structure comprises forming a first 'pad' (e.g. MOS gate) oxide layer on a first surface of a silicon substrate. An oxide etch protective layer of silicon nitride is selectively formed on a first portion of the pad oxide layer so as to overlie a first surface portion of the silicon substrate in which active device regions will be introduced. A second oxide layer is then deposited on the pad oxide layer and on the nitride layer. The dual oxide layer is then patterned to form a trench mask which exposes a second surface portion of the silicon substrate. An etchant is then applied to the structure so as to etch away material from the silicon substrate exposed by the second surface portion and a portion of the second oxide layer, thereby forming a trench in the second surface portion of the silicon substrate. After any remaining portion of the second oxide layer is removed, local oxidation of the structure is performed so as to form a third oxide layer in the trench and a field oxide at surface portions of the substrate adjacent to the nitride layer. A layer of polysilicon is non-selectively deposited over the entire structure to fill the oxide-lined trench and then polished down to the nitride layer which serves as a polishing stop. The nitride is then stripped off the pad oxide in preparation for device region processing.

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC | Draw Desc | Image |

☐ 6. Document ID: DE 4127925 A1

L6: Entry 6 of 6   File: EPAB   Feb 25, 1993

DOCUMENT-IDENTIFIER: DE 4127925 A1
TITLE: Mfr. of insulating, monocrystalline silicon@ island for microelectronic IC - by oxygen implanting doped monocrystalline silicon@ region, depositing epitaxial silicon@ layer, forming trench, forming ma

Abstract (1):
Insulated, monocrystalline silicon island is mfd. by 1) oxygen implantating in a monocrystalline Si region (1) which is lightly- or moderately doped, to form a buried, insulated SiO2 layer (2); 2) annealing the layer structure (1,2,3) produced; 3) depositing a monocrystalline epitaxial Si layer (4); 4) producing a trench etching mask (5) on the epitaxial Si layers; 5) defining the trench by photolithography; 6) etching the trench as far as the buried, insulating SiO2 layer (2) which serves as an etch stop; 7) filling the trench; 8) producing a mask on the rear face of the Si wafer; 9) locally opening the mask using photolithography; and 10) etching the Si (1) from the rear face of the Si wafer through the local opening in the mask to the buried, insulating SiO2 layer (2) serving as the etch stop. USE/ADVANTAGE - The insulated Si island can be incorporated without problems in mfg. processes for microelectronic integrated circuits, and has improved electrical and thermal insulation. The mask on the rear face is silicon oxide or silicon nitride. The trench is filled with polycrystalline Si or with oxide. Boron or arsenic are used as the dopants for the trench sidewalls. The trench etch mask is produced by i) the deposition or thermal growth of an oxide layer (5); ii) the deposition of a nitride layer (6); and iii) the deposition of an oxide layer. The Figure is a cross-section through a semiconductor wafer in the early stages of mfr. Oxygen implantation is effected on the doped substrate 1 to produce a buried, insulating SiO2 layer 2, which defines the n-type Si layer 3. The layer system 1,2,3 is then thermally annealed to convert the n-type Si layer 3 to a high-quality monocrystalline layer. An epitaxial Si layer 4, with a thickness of 1-10 microns, is then deposited, followed by a pad oxide layer 5, a nitride layer 6 which acts as a diffusion barrier, and a final oxide layer 7.

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC | Draw Desc | Image |

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Terms	Documents
semiconductor and (trench or groove) and pad and mask and etch	6

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